Remarks

This Amendment is filed in response to the final Office Action dated October 22, 2003, which has a shortened statutory period set to expire January 22, 2004. Applicants respectfully submit that Claims 1-20, as amended, are patentable over the cited art.

Specifically, Claim 1 recites:

a) placing cells of a circuit design by use of non-direct timing driven processes;
b) providing routing information associated with said cells;
c) performing an incremental placement of said cells using said routing information;
d) placing said cells by use of direct timing driven placement processes; and
e) repeating b) and c) after d) to optimize placement of said cells.

Applicants respectfully submit that Groenveld fails to disclose or suggest these limitations. Specifically, Groenveld teaches that a single detailed placement 245 (Col. 6, lines 49-51) is performed after a coarse placement step that need not be timing driven (Col. 7, lines 20-22) and an electrical optimization step that includes satisfying predetermined timing constraints (Col. 6, lines 8-10).

The Office Action characterizes col. 16, lines 11-27 as teaching step c). Applicants traverse this characterization. Specifically, col. 16, lines 11-27 teach that bucket equalization step 235 (Fig. 2) will change the position of cells, thereby changing the global routing and detailed routing data. This change in the position of some cells corresponds with coarse placement, not detailed placement. As explained by Goenveld, coarse placement includes assigning each cell to a specific bucket. Col. 5, lines 59-63. Bucket equalization step 235 changes the positions of some of the cells. Col. 6, lines

31-33. Therefore, bucket equalization step 235 fails to teach performing an incremental placement of cells.

The Office Action characterizes col. 3, lines 18-24 as teaching step d). Applicants traverse this characterization. Specifically, col. 3, lines 18-24 teach timing driven routing at selected stages in the design process so as to optimize routing and placement results. The placement and routing results are further optimized since detailed placement is adapted based on the fixed positions of the global routes. Applicants submit that this passage in general teaches step 240 (perform timing-driven global routing) being performed before step 245 (perform detailed placement). Therefore, this passage fails to teach repeating steps b) and c) after d).

Because Groenveld fails to disclose or suggest Applicants' recited method for placing circuit elements on an integrated circuit, Applicants request reconsideration and withdrawal of the rejection of Claim 1.

Claim 2 depends from Claim 1 and therefore is patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claim 2.

Claim 3 recites:

a) placing cells of a circuit design by use of non-direct timing driven processes;
b) routing wiring to connect said cells, thereby generating a layout;
c) minimizing required signal timing within said layout;
d) performing an incremental placement of said cells;
e) placing said cells by use of direct timing driven placement processes; and
f) repeating b), c), and d) after e) to optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or suggest these limitations for at least the same reasons presented for Claim 1. Based at least on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 3.

Claims 4-7 depends from Claim 3 and therefore are patentable for at least the reasons presented for Claim 3. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 4-7.

Claim 8 recites:

a) placing cells of a circuit design by use of non-direct timing driven processes;
b) routing wiring to connect said cells, thereby generating a layout;
c) synthesizing said layout to optimize timing;
d) performing an incremental placement of said cells based on said synthesizing;
e) placing said cells by use of direct timing driven placement processes; and
f) repeating b), c), and d) after e) to optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or suggest these limitations for at least the same reasons presented for Claim 1. Based at least on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 8.

Claims 9-11 depends from Claim 8 and therefore are patentable for at least the reasons presented for Claim 8. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 9-11.

Claim 19, as amended, now recites:

a processor coupled to a bus;

a memory coupled to said bus and wherein said memory contains instructions that when executed implement a method for placing circuit elements on an integrated circuit, said method comprising the steps of:

a) placing cells of a circuit design without regard to circuit timing;

b) providing routing information associated with said cells;

c) performing a detailed placement of said cells using said routing information;

d) placing said cells by use of direct timing driven placement processes; and

e) repeating b) and c) after d) to optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or suggest these limitations for at least the same reasons presented for Claim 1. Based at least on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 19.

Claim 20 depends from Claim 19 and therefore is patentable for at least the reasons presented for Claim 19. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claim 20.

Applicants are confused by the citation of U.S. Patent 5,218,551 (Agrawal), which is not used in the detailed rejection of the claims, but is briefly discussed in the Office Action, paragraph 17. Fig. 8 of Agrawal teaches a circuit migration process 800 that alleviates timing problems indicated by slack values of the changed paths. Col. 18, lines 49-52. In process 800, groups of blocks can be moved from one precinct to another on the same net. Col. 18, lines 65-68. Col. 19, lines 3-33 teach exemplary block moves between precincts.

Applicants are unclear why Agrawal is being cited in the Office Action. Applicants respectfully submit that Agrawal fails to remedy the deficiencies of Groeneveld.

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Request For A Telephone Interview

If the Examiner's next action is other than allowance of Claims 1-11 and 19-20, Applicants request a telephone interview to clarify any remaining issues in the case. To schedule this telephone interview, please contact Jeanette Harms at 408-451-5907.

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CONCLUSION

Claims 1-20 are pending in the present Application. Applicants respectfully request allowance of these claims.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION (37 C.F.R. 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being transmitted by facsimile to the Patent and Trademark Office.

Date: 12/10/03 Signature: Rebecca A Baumann